UWB Non-Coherent High Data Rates Transceiver Architecture and Implementation

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***Abstract*— Various methods of using the UWB spectrum have been developed to date, characterized by specific modulation schemes, such as MBOA or DS-UWB modulation. A new method emerging today utilizes a non coherent energetic multi-band approach, where information is encoded with the presence or not of energy in a frequency sub-band. One of the challenge in UWB communication system is the hardware design on the high operating frequencies (3.1-10.6 GHz). The low consumption, low cost and integration capability is also a challenge for designers. Transceiver architectures of this new energy frequency divison multiplex modulation are described and an overview of implementation functions are presented.**

***Index Terms*— UWB, Non-coherent Detection, OOK, RF Design, Frequency Division Multiplexing.**

I Introduction

Considering Ultra Wide Band (UWB) radio link, in accordance with the American Federal Communications Commission (FCC) regulation [1], we aim at studying a new method of using the UWB spectrum. This new method is presented in [2] and consists in an On-Off Keying (OOK) modulation generalized over multiple frequency sub-bands. The demodulation is based on a non-trivial energetic threshold comparison and described below.

Favoring non-coherent demodulation, and thus a receiver working as an energy detector, information is preferably carried by signal amplitude rather than its phase. It naturally leads to consider Pulse Amplitude Modulation (PAM). In that case an OOK modulation appears to be a suitable candidate since it possesses a good optimality considering a non-coherent demodulation [4]. To increase the system capacity, it is proposed to duplicate this basic scheme on several separate frequency sub-bands (in practice from 8 to 24) [2]. The adopted non-coherent receiver structure per sub-band is composed of a band-pass filter, a square law device and a gate integrator as shown in Fig. 1. Integration time T_i and pulse repetition

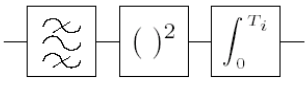

Fig. 1. Non-coherent receiver: energy integration

period T_r, will be roughly chosen considering the channel delay spread T_d as shown Fig. 2.

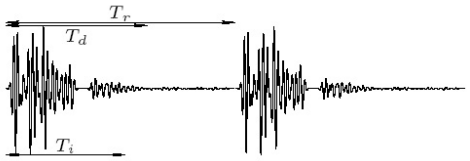

Fig. 2. Repetition time, delay spread and integration time

From the receiver point of view, the sub-band demodulation stage exacts to face the two following hypotheses [2]:

$$\begin{cases} H_0 = \int_0^{T_i} [n_k(t)]^2 dt & (bit \quad 0) \\ H_1 = \int_0^{T_i} [s_k(t) + n_k(t)]^2 dt & (bit \quad 1) \end{cases} \tag{1}$$

where, $s_k(t)$ is the deterministic signal while $n_k(t)$ corresponds to the noise, each of them filtered in the k^{th} sub-band. With respect to the integrator output x, the demodulation stage consists in deciding "at best" between H_0 and H_1, i.e intending to minimize the error probability comparing the statistic x to a predefined threshold γ_{opt} and deciding according to:

$$x \underset{H_1}{\overset{H_0}{\lessgtr}} \gamma_{opt} \tag{2}$$

where γ_{opt} is the solution of $p_0(x) = p_1(x)$ assuming equal probability likely bits 0 and 1, $p_i(x)$ being the probability density function under the hypothesis $(H_i)_{i\in[0,1]}$. It was shown that using a prior information made of the approximate channel delay spread and the available energy level allows the non-coherent system to reach high performances using a semi analytical computation of γ_{opt} (for more details please see [2] and [3]).

In Table. I from [2], numerical results of three link budget samples are presented. P_e is the mean of the error probability

TABLE I
Performances samples

Bit Rate	150	240	600	Mbit/s
P_e	10^{-5}	10^{-5}	10^{-5}	
d	10	5	3	m
N_{band}	12	12	24	
B	500	500	250	MHz
T_r	80	50	40	ns
T_i	50	40	30	ns
CM	4	3	2	

according to IEEE 802.15.3a error probability calculation proposal [5]. d is the distance between receiver and transmitter, and CM, are IEEE 802.15.3a channel models [5]. The CM types 2, 3 and 4 are all NLOS (Non Line Of Sight) and respectively valid from 0 to 4 meters, from 4 to 10 meters and for extreme multi path configurations. Data rates are computed without channel coding.

Due to its non-coherent nature, the system described here needs 3 to 5 more decibels than a coherent receiver to achieve the same performance. On the other hand, since it is able to recover almost 100% of the available energy, it means that a coherent receiver should collect at least 40% of each emitted pulse's energy to yield the same results. With such a spreading channel as the UWB channel is (see Fig. 2), doing so would require to use a RAKE receiver with lots of fingers. As shown by propagation measurements [5], the number of significant paths can be up to 60 to recover 85% of available energy.

In this paper we present results related to the hardware implementation of these non-coherent principles.

II Transceiver Architecture

II-A Transmitter

Transmitter implementation sketches are presented in Fig. 3, 4. The first solution uses a band-pass filter bank of up to n adjacent filters (Fig. 3). At the input of this filter bank, a UWB pulse (covering the whole 3.1 - 10.6 GHz bandwidth) is generated with a repetition period T_r. On each line, the relatively narrow-band pulses (from 250 to 500 MHz according to Table. I) are modulated by an OOK modulation at the rate of $1/T_r$. Once modulated, every "narrow-band" pulses are combined before being sent through an UWB antenna. Difficulties of this implementation are the wide-band pulse generation energy splitter, and combiners designs. For example this scheme needs a 100 ps mother pulse width, centered on 6.85 GHz to cover at least the whole 3.1 - 10.6 GHz bandwidth. Thus, the first energy splitter stage have to put up with all the bandwidth and a complex amplification scheme must be determined to equalize all the sub band energy in order to occupy optimally the spectrum mask according to local requirements.

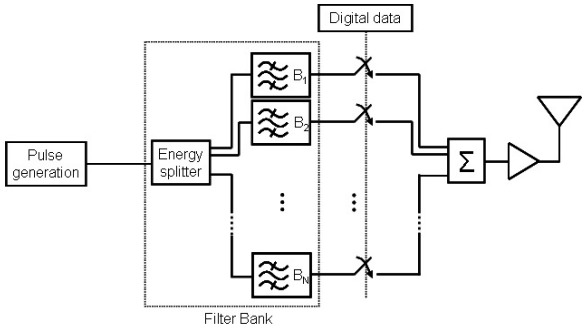

Fig. 3. Transmitter implementation sketch 1

Conversely, a second solution using an hybrid ($N \times M$) implementation is illustrated Fig. 4. This scheme uses a bank of M pulsers and M antennas, each pulser (resp. antenna) connected to an order N band-pass filter bank. In this solution the constraint on the mother pulse width to generated is relaxed, wide signal is produced only behind the adder relaxing design complexity. The system needs on each cell a $7.5/M$ GHz bandwidth mother pulse centered on $3.1 + (2k+1)\ \frac{7.5}{2M}$GHz $, k = 0 \ldots M-1$. So splitter, adder, amplifier and antenna have to put up with this relax bandwith constraints.

For example we propose a (4×6) (see Fig. 12) scheme that allows a $(10.6 - 3.1)/4 = 1.875$ GHz bandwidth requirement for RF stage. We propose a filter bank with 6 band-pass filters that permit 600 Mbit/s data rate in Table. I conditions. So this implementation relaxes pulse generation, adder and splitter constraints.

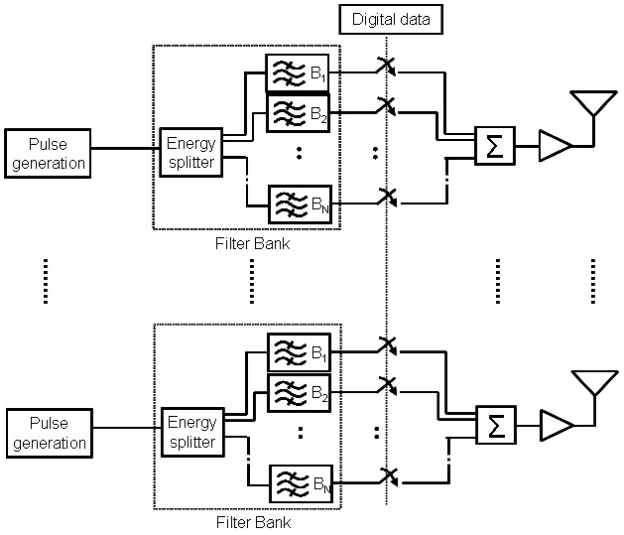

Fig. 4. Hybrid ($N \times M$) Transmitter implementation

II-B Receiver

Two receiver implementation sketches are presented Fig. 5 and Fig. 6. A band-pass filter bank splits the signal on demodulation lines. Then on each parallelized stage, a square law device and an integrator follow the output, which is sampled at a rate of $1/T_r$. The difference between the two implementations is the antenna and the first RF stage designs.

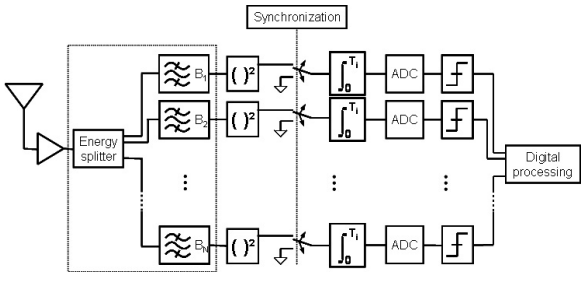

Fig. 5. Receiver implementation sketch

The first solution (Fig. 5) uses a single antenna. The splitter first stage and the LNA (Low Noise Amplifier) have to put up with the whole bandwidth (i.e 7.5 GHz). Unlike, the second implementation presents a multi-antenna design which

allows the splitter cancellation and relaxed LNA bandwidth. An hybrid solution based on multi-antenna and splitter (one antenna for N frequency sub-bands) may be optimal. This scheme is composed of M antennas, M LNA and one filter bank connected to N demodulation line (see Fig. 12 for a (4×6) hybrid architecture).

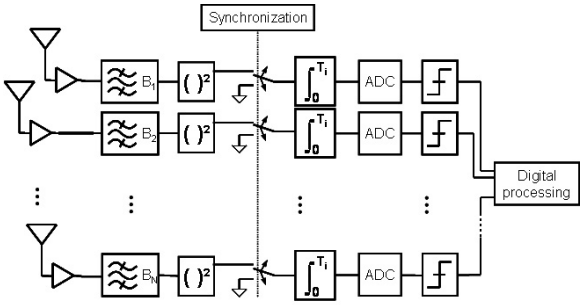

Fig. 6. Receiver implementation sketch 2

Other solutions based on baseband transposition are also possible. Their major drawback is the use of local oscillators which may introduce energy deviation. Because the modulation is based on the energy detection, energy deviation may interfere with the useful signal and bias performances.

III Implementation

The hardware implementation greatly benefits from the relaxed constraints offered by the asynchronous approach. Primarily, only a coarse synchronization is needed, which makes the system robust against the clock jitter and every triggering inaccuracy. Secondly, since the treatment is based on energy, the transceiver performances are nearly insensitive to distortion and phase non-linearity of devices like antennas, amplifiers or filters. Finally, a low power consumption is achieved thanks to the use of mainly analog and passive devices.

This section describes implementation issue for basic functions: pulser, splitter, gate integrator, switch and square law device.

III-A Pulser

Pulse generation and pulse detection in the sub-nanosecond time domain is a manifold topic. There are many possibilities of pulse generation by using special semiconductor devices like step recovery diodes and avalanche transistors, emitter coupled logic (ECL), or by using the rise time of modern ultra fast logic [6].

According to transmitter strategy, the constraint on pulse width to generate may be relaxed. For example, the design of a pulser for the (4×6) hybrid architecture above mentioned (Fig. 12) does not seem to be a real challenge. Using baseband generation, it needs 2 ns for 500 MHz bandwidth. For consumption and integrability requirements, it seems that a ultra-fast logic implementation for pulser is the most appropriated solution. Pulses are baseband generated and local oscillators ensure the frequency transposition toward each "narrow-band". Notice that oscillators are only used to provide transposition, coherence is not required.

III-B Splitter

Basic energy splitters (like Wilkinson [7]) consist in a power division. An input signal is divided by the splitter into two (or more) signals of less power levels. For a two way Wilkinson divider, the power at each filter input is being halved. For our application this type of splitters are not optimal for consumption point of view.

So the purpose is to divide the frequency band into a number of channels to preserve each sub-band power. This is the frequency multiplexer behavior. Indeed a diplexer separates the frequency band into two parts. A common way to realize a multiplexer is to combine different diplexers.

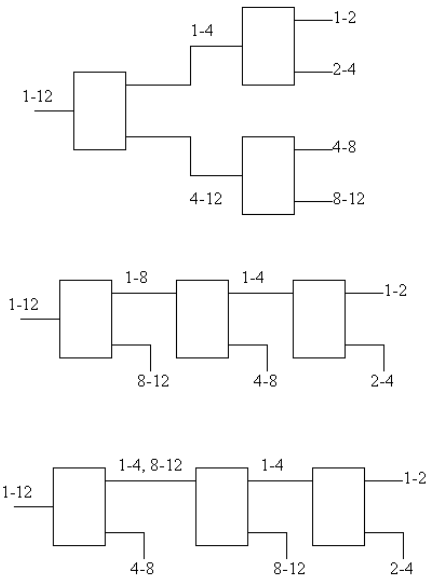

Fig. 7. Three different connections of diplexers to form a multiplexer

Fig. 7 shows three different ways of connecting three diplexers to split the frequency band (1 to 12 GHz) into sub-bands (1 to 2), (2 to 4), (4 to 8) and (8 to 12 GHz). While all three methods will yield satisfactory performance, all three of the filters shown in the first two configurations are required to have the cross-over performance demanded by the design specifications, which would most probably call for high selectivity filters. On the other hand, in case of the last configuration, the center filter that splits the band (1 to 4, 8 to 12) into the bands (1 to 4) and (8 to 12) requires only very gradual response characteristic in the changeover region, in which case a very low order diplexer would suffice.

By application of lumped components transformations like the Richard's ones, a diplexer can be easily design using the complementary filters defined in [8]. However this transformations are very difficult to realize. So we propose a method using 3 ports circulators and filters to simply design basic diplexer. A complete multiplexer is currently under studying. This muliplexer shown Fig. 8 is constructed with quadrature $(90°)$ hybrids [7] that allows simple and low cost design.

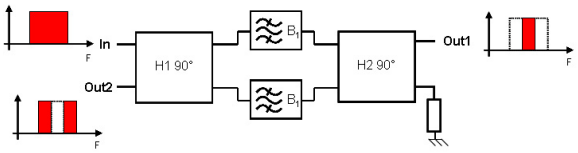

Fig. 8. A diplexer designed with quadrature (90°) hybrids and two identical band-pass filters

III-C Square law devices

A square law device is not easy to design with wide bandwidth constraint. Diodes are the better components that offer wide bandwidth, and non linearity function as square law. Diode detectors can be used as square law device [9].

Diode detectors are used to detect small signals close to the noise level and to monitor large signals well above the noise. From the noise level up to about -20 dBm the slope of the response curves is constant (see Fig. 9). This is the square law region. The diode receives the signal directly from the antenna in most systems, although a preamplifier may be used to improve sensitivity. So using zero bias diode, the device is low cost and low power consumption. This type of receiver is used in short range radar or in counter-measure equipment where the sensitivity of the more complicated superheterodyne receiver is not needed [9].

The diode detection law, over a wide range of input power level P_{in}, follows the formula:

$$V_{out} = K(\sqrt{P_{in}})^{\alpha} \tag{3}$$

where V_{out} is the detector output voltage and α is the detection law. At low level, in square law region, $\alpha \approx 2$. So the aim of the detector diode is to convert input RF power to output voltage. A typical transfer curve for a Schottky detector diode is shown in Fig. 9. At low power levels, the transfer

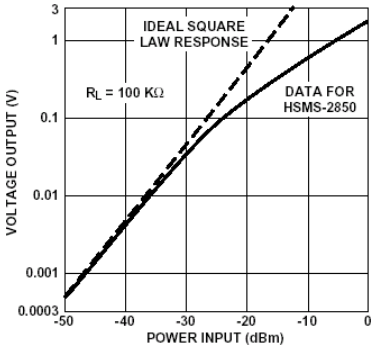

Fig. 9. Typical detector transfer curve from [9]

characteristic of a Schottky diode follows a square-law rule, with voltage output proportional to power (voltage squared) input. As input power is increased, the slope of the V_{out}/P_{in} curve flattens out to more nearly approximate a linear (voltage output proportional to RF voltage input) response.

Let's note that at both low and high temperature, temperature dependence can lead to degradation in performance. [9] and [10] present temperature compensated diode detector circuit for square law device.

III-D Gate integrators

First, on each parallelized stage, integrator device may be the same baseband component whose bandwidth is defined by twice the bandwidth of the above band pass filter. Considering an OOK modulated signal $S(t)$ which is band-pass filtered, the filter output signal $S_F(t)$ is equal to:

$$S_F(t) = S(t) * h_F(t) = r(t)\cos(2\pi f_0 t) \tag{4}$$

where $h_F(t)$ is the bandpass filter transfer function (band B, central frequency f_0) and $r(t)$ the filtered signal envelope of bandwith B. After the square law operation:

$$S_{FQ}(t) = \frac{r^2(t)}{2}(1 - \cos(4\pi f_0 t)) \tag{5}$$

Considering $f_0 \gg B$, the integrator output x is:

$$x = \int_0^{T_i} S_{FQ}(t)dt \cong \frac{1}{2}\int_0^{T_i} r^2(t)dt \tag{6}$$

where T_i is the integration time. This equation shows the baseband signal $r(t)$ contains the information. So integrator component could be a baseband component which could be the same for each parallelized stage.

To realize a gate integrator, it needs a time to discharge the system at the end of the integration cycle. This discharge time may be an handicap for an integration repetition time within one clock period and continuously outputs an integrated voltage every clock period.

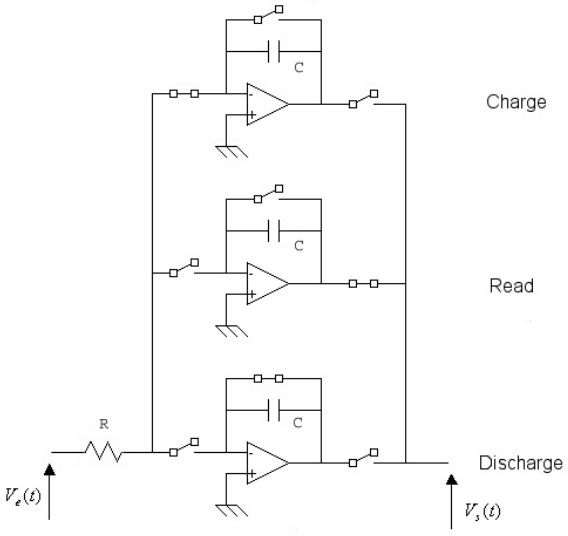

Fig. 10. Schematic design of a charge-successive integrator

So, the idea is to parallelize integration (see [11]). The integrator component is composed by three active integrators and switches. The output signal $V_s(t)$ is:

$$V_s(t) = -\frac{1}{RC}\int_t^{t+T_i} V_e(t)dt \tag{7}$$

Each integrator is operated circularly at the charge, read, or discharge state. A signal at the read state is the output and will be digitized. Fig. 10 presents a charge successive three

stage integrator. Let's note that for shorter integration time, we could parallelize integrator cells.

Another idea consists in factorizing integration operation and Analog to Digital Conversion (ADC). The architecture of a ramp convertor is modified as shown Fig. 11. First, the input signal is integrated by the first AOP cell. At the end of the integration time, the switch 1 swings to a reference voltage $-V_{REF} < 0$, the switch 3 is closed and the counter is triggered. The integration cell now integers a constant and the cell output signal is:

$$V(t) = V_{int} + \frac{V_{REF}t}{RC} \tag{8}$$

where V_{int} is the signal from port IN which has been integrated ($V_{int} < 0$). So, this equation shows that the integrated signal V_{int} is proportional to the time t. In order to compute the digital ouptut, we stop the counter when $V(t_f) = 0$.

$$V(t_f) = 0 \Rightarrow t_f = -V_{int}\frac{RC}{V_{REF}} \tag{9}$$

At the end of the integration and convertion cycle the system

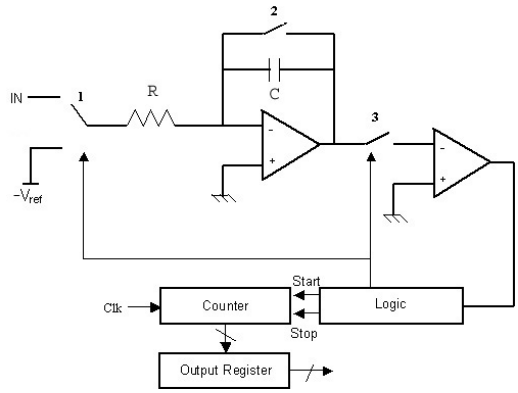

Fig. 11. Analog-to-Digital convertor with integrator operation

is reset (switch 2 is closed) in order to compute a new symbol. This cell could be parallelized for short integration time repetition.

IV Conclusion

A new architecture has been identified for the proposed modulation. It consists in a frequency sub-band division, each RF sub-bands connected to one antenna and a filter bank. The hybrid 4×6 architecture (Fig. 12) would offer the best compromise between small integration and bandwith constraints. This idea of break up frequency bandwith into several RF stage to decrease bandwith requirement, may be extended to all UWB systems using multi band approach.

We have underlined that hardware implementation greatly benefits from the relaxed constraints offered by the high data rate impulse radio transceiver. Only a coarse synchronization is needed, which makes the system robust against the clock jitter and every triggering inaccuracy. Secondly, the transceiver performances are nearly insensitive to distortion and phase non-linearity of devices like antennas, amplifiers or filters, that relaxed designers constraints.

We have highly demonstrated that this architecture use mainly analog and passive devices. Thanks to these properties we would achieve in a low cost and low power consumption. In particular, integration in small and low cost devices is easier than what could be assumed at a first glance.

Besides, relaxed synchronization methods based on time-hopped signal detection have also been investigated to enable fast channel delay spread estimation. From a system point of view, usual Medium Access Control (MAC) would be re-visited taking benefit from energy detection techniques based on the inherent flexible frequency separation properties of such a system.

This study provides many opportunities for future implementation research. Presently design a UWB prototype appears to be the next step. Fig. 12 shows a implementation issues for a future prototype.

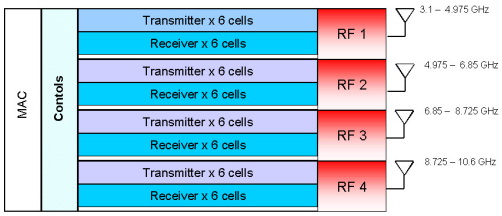

Fig. 12. Transceiver implementation sketch proposal

Acknowledgment

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